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VERIFICATION OF TRANSLATION

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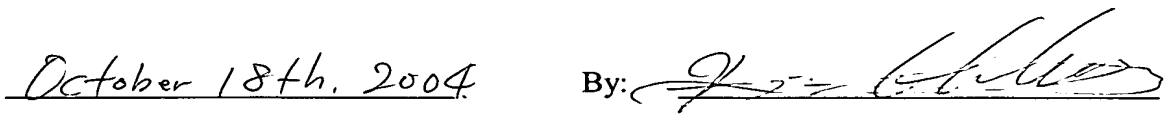
(1) I am fluent in both the Japanese and English languages;

(2) I have read both the translation of the above-identified application from Japanese to English and the original Japanese text;

(3) The English translation is a true and correct translation of the above-identified application to the best of my knowledge; and

(4) That all statements made are of my own knowledge, are true, and that all statements made on information and belief are believed to be true, and further that these statements are made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001, and that such false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: October 18th, 2004 By: 

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TESTING APPARATUS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a testing apparatus. More particularly, the present invention relates to a testing apparatus including a plurality of testing module slots onto which different types of testing modules are optionally mounted.

2. Description of the Related Art

A testing apparatus for performing an analog test of a device under test performs the test by instructing one testing module to generate and supply a test signal to the device under test and another testing module to measure the output signal from the device under test. In order to properly operate each of a plurality of testing modules, each of a plurality of controlling modules selects and supplies both a trigger signal and a clock signal in response to the type of each of the testing modules among a plurality of trigger signals and clock signals to the testing module based on a testing program. In order to realize the operations of such controlling modules, one who prepares the testing program prepares a management table for managing the connections of the inputs and outputs of the controlling modules so as to arbitrarily select the trigger signals and the clock signals inputted to the controlling modules, and the trigger signals and the clock signals outputted from the controlling modules to the testing modules, and prepares a testing program for testing the device under test in consideration of the connections of inputs and outputs of the controlling modules.

Recently, a testing apparatus including a plurality of

testing module slots onto which different types of testing modules for generating different types of test signals for the test of the device under test respectively are optionally mounted has been developed. In such testing apparatus, since the connection relation of the controlling modules and the testing modules are arbitrarily changed, and the times required for the test operations for the test modules are different from each other, it is inevitable to prepare a management program whenever the testing modules are changed, and a testing program in response to the mounting positions the testing modules whenever the testing modules are changed, and a preparation process is needed for a extremely difficult test.

SUMMARY OF THE INVENTION

Therefore, it is an object of the present invention to provide a testing apparatus, which is capable of overcoming the above drawbacks accompanying the conventional art. The above and other objects can be achieved by combinations described in the independent claims. The dependent claims define further advantageous and exemplary combinations of the present invention.

According to the first aspect of the present invention, a testing apparatus having a plurality of testing module slots onto which different types of testing modules for generating different types of test signals to test a device under test are optionally mounted, includes a plurality of controlling modules for supplying a control signal to each of the testing modules, the testing modules being mounted on the testing module slots respectively, the control signal being used for controlling the testing module, setting information supplying means for supplying

hardware setting information to a specific testing module among the testing modules, the hardware setting information being set in advance in the controlling module in order to send the control signal in response to the specific testing module, enable signal controlling means for instructing the testing module to generate and supply an enable signal to the controlling module supplying the control signal to the testing module, and setting means for setting a specific controlling module of the controlling modules to supply the control signal in response to the specific testing module to the specific testing module based on the hardware setting information, the specific controlling module receiving the enable signal from the specific testing module.

The controlling module may include a plurality of interfaces for inputting different types of the control signals respectively, the setting information supplying means may select a specific control signal among the control signals and supplies the hardware setting information to the controlling module via a specific interface among the interfaces, the specific interface inputting the specific control signal to the controlling module, and the setting means may set the controlling module to supply the specific control signal to the specific testing module, the specific control signal being inputted from the specific interface to the controlling module.

The controlling module may further include a multiplexer circuit for selecting the specific control signal to be supplied to the specific testing module among the control signals inputted from the interfaces respectively, and a flip-flop circuit for holding information indicating that the hardware setting information is inputted from the specific interface as a select signal for controlling the multiplexer circuit to select the specific control signal, based on a setting request signal supplied

from the setting means, when the enable signal is received from the specific testing module.

The control signal may be a trigger signal for controlling the testing module, and the multiplexer circuit may select and supply a trigger signal to be supplied to the specific testing module among different types of the trigger signals inputted from the interfaces respectively.

The control signal may be a clock signal for controlling the testing module, and the multiplexer circuit may select and supply a clock signal to be supplied to the specific testing module among different types of the clock signals inputted from the interfaces respectively.

The controlling module may further include a first multiplexer circuit for selecting a trigger signal to be supplied to the specific testing module among different types of trigger signals for controlling the testing modules, the trigger signal being inputted from each of the interfaces as the control signal, a first flip-flop circuit for holding information indicating that the hardware setting information is inputted from the specific interface as a select signal for controlling the first multiplexer circuit to select the trigger signal, based on a setting request signal supplied from the setting means, when the enable signal is received from the specific testing module, a second multiplexer circuit for selecting a clock signal to be supplied to the specific testing module among different types of clock signals for controlling the testing modules, the clock signal being inputted from each of the interfaces as the control signal, and a second flip-flop circuit for holding information indicating that the hardware setting information is inputted from the specific interface as a select signal for controlling the second multiplexer circuit to select the clock signal, based on a setting request

signal supplied from the setting means, when the enable signal is received from the specific testing module.

The testing apparatus may further include a first site controlling apparatus for controlling a first testing module among the testing modules, and a second site controlling apparatus for controlling a second testing module among the testing modules, wherein the enable signal controlling means may instruct the first testing module to generate and supply the enable signal to a first controlling module among the controlling modules, the first controlling module supplying the control signal to the first testing module, and the second testing module to generate and supply the enable signal to a second controlling module among the controlling modules, the second controlling module supplying the control signal to the second testing module, the setting information supplying means may supply the hardware setting information via a first interface among the interfaces, the first interface inputting the control signal generated under the control of the first site controlling apparatus to the first controlling module, and via a second interface among the interfaces, the second interface inputting the control signal generated under the control of the second site controlling apparatus to the second controlling module, and the setting means may set the first controlling module to supply the control signal to the first testing module, the control signal being inputted from the first interface to the first controlling module, and the second controlling module to supply the control signal to the second testing module, the control signal being inputted from the second interface to the second controlling module.

The testing apparatus may test a plurality of the devices under test at the same time, the enable signal controlling means may instruct a first testing module among the testing modules

to generate and supply the enable signal to a first controlling module among the controlling modules, the first testing module supplying the test signal to a first device under test among the devices under test, the first controlling module supplying the control signal to the first testing module, and a second testing module among the testing modules to generate and supply the enable signal to a second controlling module among the controlling modules, the second testing module supplying the test signal to a second device under test among the devices under test, the second controlling module supplying the control signal to the second testing module, the setting information supplying means may supply the hardware setting information via a first interface among the interfaces, the first interface inputting the control signal for controlling the test of the first device under test to the first controlling module, and via a second interface among the interfaces, the second interface inputting the control signal for controlling the test of the second device under test to the second controlling module, and the setting means may set the first controlling module to supply the control signal to the first testing module, the control signal being inputted from the first interface to the first controlling module, and the second controlling module to supply the control signal to the second testing module, the control signal being inputted from the second interface to the second controlling module.

The testing modules may be analog measuring modules for performing an analog test of the device under test, and the controlling modules may supply a control signal to each of the analog measuring modules, the control signal being used for controlling the analog measuring modules.

The summary of the invention does not necessarily describe all necessary features of the present invention. The present

invention may also be a sub-combination of the features described above. The above and other features and advantages of the present invention will become more apparent from the following description of the embodiments taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows an example of the configuration of a testing apparatus 100 related to an exemplary embodiment of the present invention.

Fig. 2 shows a first example of the configuration of a trigger controlling module 114a.

Fig. 3 shows a second example of the configuration of a trigger controlling module 114a.

Fig. 4 shows a third example of the configuration of a trigger controlling module 114a.

DETAILED DESCRIPTION OF THE INVENTION

The invention will now be described based on the preferred embodiments, which do not intend to limit the scope of the present invention, but exemplify the invention. All of the features and the combinations thereof described in the embodiment are not necessarily essential to the invention.

Fig. 1 shows an example of the configuration of a testing apparatus 100 related to an exemplary embodiment of the present invention. The testing apparatus 100 includes a controlling apparatus group 102, a plurality of trigger signal sources 104a to 104d, a plurality of clock signal sources 106a to 106d, an analog synchronization controlling unit 108, a plurality of testing modules 118a to 118c, and a plurality of testing module

slots 120a to 120c.

The controlling apparatus group 102 includes a general controlling apparatus 101 and a plurality of site controlling apparatuses 103a and 103b. The analog synchronization controlling unit 108 includes a trigger matrix 110 and a clock matrix 112. The trigger matrix 110 includes a plurality of trigger controlling modules 114a to 114c, and the clock matrix 112 includes a plurality of clock controlling modules 116a to 116c.

The testing apparatus 100 generates and supplies test signals to the devices under test 150a to 150c, measures the output signals from the devices under test 150a to 150c as the results of their operations in response to the test signals, and judges the quality of the devices under test 150a to 150c based on the measurement results. The testing apparatus 100 is realized through an open architecture, where modules based on the open architecture are used as the testing modules 118a to 118c for supplying the testing signals to the devices under test 150a to 150c. In other words, onto the testing module slots 120a to 120c, different types of testing modules 118a to 118c are optionally mounted to generate different types of testing signals for the test of the devices under test 150a to 150c respectively. The testing modules 118a to 118c are analog measurement modules for the analog test of the devices under test 150a to 150c such as arbitrary waveform adjusters for generating and supplying arbitrary analog waveforms to the devices under test 150a to 150c, and phase characteristic testers for testing the phase characteristics of their analog waveforms, by receiving the analog waveforms outputted by the devices under test 150a to 150c in response to the analog waveforms supplied from the arbitrary waveform adjusters.

Each of the trigger controlling modules 114a to 114c and the clock controlling modules 116a to 116c supplies trigger and

clock signals to the plurality of testing modules 118a to 118c in order to control the operations of the plurality of testing modules 118a to 118c mounted onto the plurality of testing module slots 120a to 120c respectively. The trigger and clock signals are an example of the controlling signals of the present invention.

The trigger controlling modules 114a to 114c include a plurality of interfaces for the inputs of a plurality of different types of trigger signals supplied from each of the trigger signal sources 104a to 104d. The clock controlling modules 116a to 116c include a plurality of interfaces for the inputs of a plurality of different types of clock signals supplied from each of the clock signal sources 106a to 106d. In addition, the trigger controlling modules 114a to 114c receive the trigger signals generated by the trigger signal sources 104a to 104d respectively, select one of the trigger signals under the control of the controlling apparatus group, and supply it to the testing modules 118a to 118c. And the clock controlling modules 116a to 116c receive the clock signals generated by the clock signal sources 106a to 106d respectively, select one of the clock signals under the control of the controlling apparatus group, and supply it to the testing modules 118a to 118c. Here, the trigger signal sources 104a to 104d and the clock signal sources 106a to 106d are, e.g. the digital synchronization controlling unit and the performance board. In addition, the testing modules 118a to 118c, the trigger controlling modules 114a to 114c or the clock controlling modules 116a to 116c may function as the trigger signal sources 104a to 104d or the clock signal sources 106a to 106d.

The general controlling apparatus 101 obtains and stores a test controlling program, a testing program, and test data used by the testing apparatus 100 to test the devices under test

150a to 150c via an external network. The site controlling apparatuses 103a and 103b function as enable signal controlling means and setting means related to the present invention, so that they control the testing modules 118a to 118c and test each of the devices under test 150a to 150c in parallel at the same time. The connection relation between the site controlling apparatuses 103a and 103b and the testing modules 118a to 118c is changed in response to the number of the pins of the devices under test 150a to 150c, the shape of the wirings of the performance board, the type of the testing modules 118a to 118c, etc., and the site controlling apparatuses 103a and 103b test the devices under test 150a to 150c in parallel. In addition, the site controlling apparatuses 103a and 103b perform different test sequences in response to the performance of the devices under test 150a to 150c. For example, the site controlling apparatus 103a controls the operations of the testing modules including the testing module 118a among the testing modules 118a to 118c, whereas the site controlling apparatus 103b controls the operations of the testing modules including the testing module 118b among the testing modules 118b to 118c. In other words, each of the site controlling apparatuses 103a and 103b divides the testing modules 118a to 118c into the sites of the number of the site controlling apparatuses 103a and 103b to control the operations of the testing modules including each of the sites.

The site controlling apparatuses 103a and 103b obtain and perform the test controlling program from the general controlling apparatus 101. Then, the site controlling apparatuses 103a and 103b obtain the testing program and the test data used for the test of the devices under test 150a to 150c from the general controlling apparatus 101 based on the test controlling program, and supply them to the testing modules 118a to 118c. Then, the

site controlling apparatuses 103a and 103b instruct the testing modules 118a to 118c to start the test based on the testing program and the test data by supplying the trigger signals generated by the trigger signal sources 104a to 104d and the clock signals generated by the clock signal sources 106a to 106d towards the testing modules 118a to 118c. And the site controlling apparatuses 103a and 103b receive an interrupt indicating that the test is completed, and inform the general controlling apparatus 101.

Accordingly, each of the trigger controlling modules 114a to 114c and the clock controlling modules 116a to 116c related to this embodiment is set in advance with regard to hardware before the test of the devices under test 150a to 150c starts, and thereby which signal among the trigger signals or the clock signals generated by the trigger signal sources 104a to 104d or the clock signal sources 106a to 106d is selected and outputted is determined.

The site controlling apparatus 103a functions as setting information supplying means, and supplies hardware setting information to be set in advance in the trigger controlling module 114a and the clock controlling module 116a in order to send the trigger and clock signals in response to a specific testing module 118a among the testing modules 118a to 118c to the specific testing module 118a. Particularly, a status signal as an example of the hardware setting information is supplied from one of the trigger signal sources 104a to 104d to the trigger controlling module 114a, whereas a status signal as an example of the hardware setting information is supplied from one of the clock signal sources 106a to 106d to the clock controlling module 116a.

In other words, a specific trigger signal among the trigger signals generated by the trigger signal sources 104a to 104d

is selected, and the status signal is supplied to the trigger controlling module 114a via a specific interface among the interfaces included in the trigger controlling module 114a which inputs the specific trigger signal to the trigger controlling module 114a, whereas a specific clock signal among the clock signals generated by the clock signal sources 106a to 106d is selected, and the status signal is supplied to the clock controlling module 116a via a specific interface among the interfaces included in the clock controlling module 116a which inputs the specific clock signal to the clock controlling module 116a.

Then, the site controlling apparatus 103a functions as enable signal controlling means of the present invention, so that it supplies an enable signal generation request to the testing module 118a via a system control bus, and instructs a specific testing module 118a to generate and supply an enable signal to the trigger controlling module 114a and the clock controlling module 116a to supply the trigger signals and the clock signals to the specific testing module 118a.

In addition, the site controlling apparatus 103a functions as setting means of the present invention, so that it sets the trigger controlling module 114a and the clock controlling module 116a having received the enable signal from the specific testing module 118a to supply the trigger signals and the clock signals in response to the specific testing module 118a to the specific testing module 118a based on the hardware setting information. Particularly, a setting request signal is supplied to the trigger controlling module 114a via the system control bus, and the hardware of the trigger controlling module 114a is set to supply the trigger signal inputted from the specific interface to the trigger controlling module 114a to the specific testing module 118a. And a setting request signal is supplied to the clock controlling

module 116a via the system control bus, and the hardware of the clock controlling module 116a is set to supply the clock signal inputted from the specific interface to the clock controlling module 116a to the specific testing module 118a.

As above, since the status signals are supplied from the trigger signal sources 104a to 104d to the trigger controlling modules 114a to 114c and from the clock signal sources 106a to 106d to the clock controlling modules 116a to 116c, and the enable signals are supplied from the testing modules 118a to 118c to the trigger controlling modules 114a to 114c and the clock controlling modules 116a to 116c, it is possible to set the connection relation of the inputs and outputs of the trigger controlling modules 114a to 114c and the clock controlling modules 116a to 116c of the trigger matrix 110 and the clock matrix 112 before the test of the devices under test 150a to 150c starts. Accordingly, although the testing modules 118a to 118c mounted onto the testing module slots 120a to 120c of the testing apparatus 100 realized by an open architecture are arbitrarily changed, it is unnecessary to prepare a management table to manage the connections of the inputs and outputs of the trigger controlling modules 114a to 114c and the clock controlling modules 116a to 116c, and to prepare a testing program in response to the mounting positions of the testing modules 118a to 118c. Therefore, the test of the devices under test 150a to 150c can start quickly, and the time required to test the devices under test 150a to 150c can be reduced.

Fig. 2 shows a first example of the configuration of a trigger controlling module 114a related to this embodiment. The trigger controlling module 114a according to this embodiment includes a multiplexer circuit 200, a priority encoder 202, and a flip-flop circuit 204. The trigger controlling module 114a

according to this embodiment controls the testing module 118a to supply the trigger signals in response to the devices under test 150a to 150c by the status information held by the flip-flop circuit 204.

First, the hardware setting of the trigger controlling module 114a before the test of the devices under test 150a to 150c starts will be described. When at least one of the trigger signal sources 104a to 104d supplies a status signal to the trigger controlling modules 114a based on an instruction of the controlling apparatus group 102, the priority encoder 202 receives the signals supplied from the trigger signal sources 104a to 104d via the interfaces, and calculates the status information indicating which trigger signal source among the trigger signal sources 104a to 104d is supplying the status signal and sends it to the flip-flop circuit 204. Then, when the testing module 118a supplies an enable signal to the flip-flop circuit 204 based on an instruction of the controlling apparatus group 102, and a setting request signal is supplied from the controlling apparatus group 102 to the flip-flop circuit 204, the flip-flop circuit 204 holds the status information supplied from the priority encoder 202 as a select signal for controlling the multiplexer circuit 200 to select the control signal. Accordingly, the hardware setting of the trigger controlling module 114a is performed, and the connections of the inputs and outputs are determined.

Next, the operation of the trigger controlling module 114a during the test of the devices under test 150a to 150c will be described. The flip-flop circuit 204 supplies the status information held before the test starts as described above to the multiplexer circuit 200 as the select signal. And when the trigger signals generated by the trigger signal sources 104a to 104d are supplied to the trigger controlling module 114a via

the interfaces based on an instruction of the controlling apparatus group 102, the multiplexer circuit 200 selects a trigger signal among the trigger signals which is supplied to a specific testing module 118a based on the select signal supplied from the flip-flop circuit 204, and supplies it to the testing module 118a.

Further, the trigger controlling modules 114b and 114c have the same configuration and function as that of the trigger controlling module 114a described above. In addition, the clock controlling modules 116a to 116c have the same configuration and function as that of the trigger controlling module 114a described above except the differences between the trigger signals and the clock signals. In other words, each of the clock controlling modules 116a to 116c includes a multiplexer circuit, a priority encoder, and a flip-flop circuit having the same configuration and function as those of the multiplexer circuit 200, the priority encoder 202, and the flip-flop circuit 204.

According to the trigger controlling module 114a of this embodiment, before the test of the devices under test 150a to 150c starts, the priority encoder 202 generates the status information, and the flip-flop circuit 204 holds it as the select signal, whereby the hardware setting of the trigger controlling modules 114a to 114c and the clock controlling modules 116a to 116c is performed, and thus the trigger signal sources 104a to 104d and the clock signal sources 106a to 106d can be properly selected in response to the testing modules 118a to 118c to perform the test.

Fig. 3 shows a second example of the configuration of a trigger controlling module 114a related to this embodiment. In the testing apparatus 100 including the trigger controlling module 114a according to this embodiment, the site controlling apparatus 103a instructs the testing module 118a for supplying the test

signal to the device under test 150a to generate and supply an enable signal to the trigger controlling module 114a supplying the trigger signal to the testing module 118a. And the site controlling apparatus 103a supplies the hardware setting information from a first interface for inputting the trigger signal to the trigger controlling module 114a to control the test of the device under test 150a. And the site controlling apparatus 103a sets the trigger controlling module 114a to supply the trigger signal inputted from the first interface to the trigger controlling module 114a to the testing module 118a. In addition, the site controlling apparatus 103a instructs the testing module 118b supplying the test signal to the device under test 150b to generate and supply an enable signal to the trigger controlling module 114b supplying the trigger signal to the testing module 118b. And the site controlling apparatus 103a supplies the hardware setting information from a second interface for inputting the trigger signal to the trigger controlling module 114b to control the test of the device under test 150b. And the site controlling apparatus 103a sets the trigger controlling module 114b to supply the trigger signal inputted from the second interface to the trigger controlling module 114b to the testing module 118b.

In other words, the trigger controlling module 114a according to this embodiment includes a multiplexer circuit 300, a priority encoder 302, a flip-flop circuit 304, a flip-flop circuit 306, and a plurality of AND circuits 308a to 308d. And the trigger controlling module 114a according to this embodiment is controlled to supply the trigger signal whose type corresponds to the type of the devices under test 150a to 150c to the testing module 118a based on the status information held by the flip-flop circuit 306, and to supply the trigger signal whose type corresponds

to the testing modules 118a to 118c to the testing module 118a based on the status information held by the flip-flop circuit 304.

First, the hardware setting of the trigger controlling modules 114a before the test of the devices under test 150a to 150c starts will be described. When at least one of the trigger signal sources 104a to 104d supplies a status signal in response to the type of the device 150a to be tested by the testing module 118a to the trigger controlling module 114a based on an instruction of the controlling apparatus group 102, the signal is inputted to the flip-flop circuit 306. And when the testing module 118a supplies an enable signal to the flip-flop circuit 306 based on an instruction of the controlling apparatus group 102, and the controlling apparatus group 102 supplies a setting request signal to the flip-flop circuit 306, the flip-flop circuit 306 holds the signals supplied from the trigger signal sources 104a to 104d as the status information which is the information to select the trigger signal in response to the type of the device under test 150a based on the setting request signal.

In addition, when at least one of the trigger signal sources 104a to 104d supplies a status signal in response to the testing module 118a to the trigger controlling module 114a based on an instruction of the controlling apparatus group 102, the signal is inputted to the AND circuits 308a to 308d. And the flip-flop circuit 306 inputs the held status information to the AND circuits 308a to 308d based on the setting request signal supplied from the controlling apparatus group 102. Each of the AND circuits 308a to 308d logically multiplies each signal being supplied from the trigger signal sources 104a to 104d by the status information inputted from the flip-flop circuit 306, and supplies the result to the priority encoder 302. In other words, the

AND circuits 308a to 308d logically multiplies a plurality of status signals supplied to the trigger controlling module 114a in response to the device under test 150a by a plurality of status signals supplied to the trigger controlling module 114a in response to the device under test 150a, and supply the results to the priority encoder 302.

And the priority encoder 302 receives the operation results of the status signals supplied from the AND circuits 308a to 308d, and calculates and supplies the status information to the flip-flop circuit 304, where the status information indicates which trigger signal source among the trigger signal sources 104a to 104d is supplying the status signal in response to the type of the device under test 150a and the status signal in response to the device under test 150a. Then when the testing module 118a supplies an enable signal to the flip-flop circuit 304 based on an instruction of the controlling apparatus group 102, and the controlling apparatus group 102 supplies a setting request signal to the flip-flop circuit 304, the flip-flop circuit 304 holds the status information being supplied from the priority encoder 302 as the select signal to control the multiplexer circuit 300 to select the control signal based on the setting request signal. Accordingly, the hardware setting of the trigger controlling module 114a is performed, and the connections of the inputs and outputs are determined.

Next, the operation of the trigger controlling module 114a during the test of the devices under test 150a to 150c will be described. The flip-flop circuit 304 supplies the status information held before the test starts as described above to the multiplexer circuit 300 as the select signal. And when the trigger signals generated by the trigger signal sources 104a to 104d are supplied to the trigger controlling module 114a via

the interfaces based on an instruction of the controlling apparatus group 102, the multiplexer circuit 300 selects a trigger signal among the trigger signals which is supplied to a specific testing module 118a based on the select signal supplied from the flip-flop circuit 304, and supplies it to the testing module 118a.

Further, the trigger controlling modules 114b and 114c have the same configuration and function as that of the trigger controlling module 114a described above. In addition, the clock controlling modules 116a to 116c have the same configuration and function as that of the trigger controlling module 114a described above except the differences between the trigger signals and the clock signals. In other words, each of the clock controlling modules 116a to 116c includes a multiplexer circuit, a priority encoder, a flip-flop circuit, a flip-flop circuit, and a plurality of AND circuits having the same configuration and function as those of the multiplexer circuit 300, the priority encoder 302, the flip-flop circuit 304, the flip-flop circuit 306, and the AND circuits 308a to 308d.

According to the trigger controlling module 114a of this embodiment, before the test of the devices under test 150a to 150c starts, the flip-flop circuit 306 and the priority encoder 302 generate the status information, and the flip-flop circuit 304 holds it as the select signal, whereby the hardware setting of the trigger controlling modules 114a to 114c and the clock controlling modules 116a to 116c can be performed. And the trigger signal sources 104a to 104d and the clock signal sources 106a to 106d can be properly selected in response to the type of the devices under test 150a to 150c and the testing modules 118a to 118c to perform the test.

Fig. 4 shows a third example of the configuration of a trigger controlling module 114a related to this embodiment. In

the testing apparatus 100 including the trigger controlling module 114a according to this embodiment, the controlling apparatus group 102 instructs the testing module 118a included in a first site controlled by the site controlling apparatus 103a to generate and supply an enable signal to the trigger controlling module 114a supplying the trigger signal to the testing module 118a. And the controlling apparatus group 102 supplies the hardware setting information from a first interface for inputting the trigger signal generated on the basis of the control of the site controlling apparatus 103a to the trigger controlling module 114a to control the test of the device under test 150a. And the controlling apparatus group 102 sets the trigger controlling module 114a to supply the control signal inputted from the first interface to the trigger controlling module 114a to the testing module 118a. In addition, the controlling apparatus group 102 instructs the testing module 118b included in a second site controlled the site controlling apparatus 103b to generate and supply an enable signal to the trigger controlling module 114b supplying the trigger signal to the testing module 118b. And the controlling apparatus group 102 supplies the hardware setting information generated on the basis of the control of the site controlling apparatus 103b from a second interface for inputting the trigger signal to the trigger controlling module 114b. And the controlling apparatus group 102 sets the trigger controlling module 114b to supply the control signal inputted from the second interface to the trigger controlling module 114b to the trigger controlling module 114b.

Further, the site controlling apparatus 103a instructs the testing module 118a for supplying the test signal to the device under test 150a to generate and supply an enable signal to the trigger controlling module 114a supplying the trigger

signal to the testing module 118a. And the site controlling apparatus 103a supplies the hardware setting information from a first interface for inputting the trigger signal to the trigger controlling module 114a to control the test of the device under test 150a. And the site controlling apparatus 103a sets the trigger controlling module 114a to supply the trigger signal inputted from the first interface to the trigger controlling module 114a to the testing module 118a. In addition, the site controlling apparatus 103b instructs the testing module 118b supplying the test signal to the device under test 150b to generate and supply an enable signal to the trigger controlling module 114b supplying the trigger signal to the testing module 118b. And the site controlling apparatus 103b supplies the hardware setting information from a second interface for inputting the trigger signal to the trigger controlling module 114b to control the test of the device under test 150b. And the site controlling apparatus 103b sets the trigger controlling module 114b to supply the trigger signal inputted from the second interface to the trigger controlling module 114b to the testing module 118b.

In other words, the trigger controlling module 114a according to this embodiment includes a multiplexer circuit 400, a priority encoder 402, a flip-flop circuit 404, a flip-flop circuit 406, a plurality of AND circuits 408a to 408d, a flip-flop circuit 410, and a plurality of AND circuits 412a to 412d. And the trigger controlling module 114a according to this embodiment is controlled to supply the trigger signal whose type corresponds to the type of the site controlling apparatuses 103a and 103b to the testing module 118a based on the status information held by the flip-flop circuit 410, the trigger signal whose type corresponds to the type of the devices under test 150a to 150c to the testing module 118a based on the status information held by the flip-flop circuit

306, and the trigger signal whose type corresponds to the testing modules 118a to 118c to the testing module 118a based on the status information held by the flip-flop circuit 404.

First, the hardware setting of the trigger controlling modules 114a before the test of the devices under test 150a to 150c starts will be described. When at least one of the trigger signal sources 104a to 104d supplies a status signal in response to the type of the site controlling apparatus 103a to the trigger controlling module 114a based on an instruction of the controlling apparatus group 102, the signal is inputted to the flip-flop circuit 410. And when the testing module 118a supplies an enable signal to the flip-flop circuit 410 based on an instruction of the controlling apparatus group 102, and the controlling apparatus group 102 supplies a setting request signal to the flip-flop circuit 410, the flip-flop circuit 410 holds the signals supplied from the trigger signal sources 104a to 104d as the status information which is the information to select the trigger signal in response to the type of the site controlling apparatus 103a based on the setting request signal.

In addition, when at least one of the trigger signal sources 104a to 104d supplies a status signal in response to the type of the device under test 150a to the trigger controlling module 114a based on an instruction of the controlling apparatus group 102, the signal is inputted to the AND circuits 412a to 412d. And the flip-flop circuit 410 inputs the held status information to the AND circuits 412a to 412d based on the setting request signal supplied from the controlling apparatus group 102. Each of the AND circuits 412a to 412d logically multiplies each signal being supplied from the trigger signal sources 104a to 104d by the status information inputted from the flip-flop circuit 406, and supplies the result to the flip-flop circuit 406. In other

words, the AND circuits 412a to 412d logically multiplies a plurality of status signals supplied to the trigger controlling module 114a in response to the type of the site controlling apparatus 103a by a plurality of status signals supplied to the trigger controlling module 114a in response to the type of the device under test 150a, and supply the results to the flip-flop circuit 406.

And when the testing module 118a supplies an enable signal to the flip-flop circuit 406 based on an instruction of the controlling apparatus group 102, and a setting request signal is supplied from the controlling apparatus group 102 to the flip-flop circuit 406, the flip-flop circuit 406 holds the signals supplied from the AND circuits 412a to 412d as the status information which is the information to select the trigger signal in response to the types of the site controlling apparatus 103a and the device under test 150a based on the setting request signal.

In addition, when at least one of the trigger signal sources 104a to 104d supplies a status signal in response to the testing module 118a to the trigger controlling module 114a based on an instruction of the controlling apparatus group 102, the signal is inputted to the AND circuits 408a to 408d. And the flip-flop circuit 406 inputs the held status information to the AND circuits 408a to 408d based on the setting request signal supplied from the controlling apparatus group 102. Each of the AND circuits 408a to 408d logically multiplies each signal being supplied from the trigger signal sources 104a to 104d by the status information inputted from the flip-flop circuit 406, and supplies the result to the priority encoder 402. In other words, the AND circuits 408a to 408d logically multiplies the result of logically multiplying a plurality of status signals supplied to the trigger controlling module 114a in response to the type

of the site controlling apparatus 103a by a plurality of status signals supplied to the trigger controlling module 114a in response to the type of the device under test 150a by a plurality of status signals supplied to the trigger controlling module 114a in response to the device under test 150a, and supply the results to the priority encoder 402.

And the priority encoder 402 receives the operation results of the status signals supplied from the AND circuits 408a to 408d, and calculates and supplies the status information to the flip-flop circuit 404, where the status information indicates which trigger signal source among the trigger signal sources 104a to 104d is supplying the status signal in response to the type of the site controlling apparatus 103a, the status signal in response to the type of the device under test 150a, and the status signal in response to the testing module 118a. Then when the testing module 118a supplies an enable signal to the flip-flop circuit 404 based on an instruction of the controlling apparatus group 102, and the controlling apparatus group 102 supplies a setting request signal to the flip-flop circuit 404, the flip-flop circuit 404 holds the status information being supplied from the priority encoder 402 as the select signal to control the multiplexer circuit 400 to select the control signal based on the setting request signal. Accordingly, the hardware setting of the trigger controlling module 114a is performed, and the connections of the inputs and outputs are determined.

Next, the operation of the trigger controlling module 114a during the test of the devices under test 150a to 150c will be described. The flip-flop circuit 404 supplies the status information held before the test starts as described above to the multiplexer circuit 400 as the select signal. And when the trigger signals generated by the trigger signal sources 104a

to 104d are supplied to the trigger controlling module 114a via the interfaces based on an instruction of the controlling apparatus group 102, the multiplexer circuit 400 selects a trigger signal among the trigger signals which is supplied to a specific testing module 118a based on the select signal supplied from the flip-flop circuit 404, and supplies it to the testing module 118a.

Further, the trigger controlling modules 114b and 114c have the same configuration and function as that of the trigger controlling module 114a described above. In addition, the clock controlling modules 116a to 116c have the same configuration and function as that of the trigger controlling module 114a described above except the differences between the trigger signals and the clock signals. In other words, each of the clock controlling modules 116a to 116c includes a multiplexer circuit, a priority encoder, a flip-flop circuit, a flip-flop circuit, a plurality of AND circuits, a flip-flop circuit, a plurality of AND circuits and having the same configuration and function as those of the multiplexer circuit 400, the priority encoder 402, the flip-flop circuit 404, the flip-flop circuit 406, the AND circuits 408a to 408d, the flip-flop circuit 410, and the AND circuits 412a to 412d.

According to the trigger controlling module 114a of this embodiment, before the test of the devices under test 150a to 150c starts, the flip-flop circuit 410, the flip-flop circuit 406 and the priority encoder 402 generate the status information, and the flip-flop circuit 404 holds it as the select signal, whereby the hardware setting of the trigger controlling modules 114a to 114c and the clock controlling modules 116a to 116c can be performed. And the trigger signal sources 104a to 104d and the clock signal sources 106a to 106d can be properly selected in response to the type of the site controlling apparatuses 103a

and 103b, the type of the devices under test 150a to 150c and the testing modules 118a to 118c to perform the test.

As above, according to the testing apparatus 100 of this embodiment realized by an open architecture, although the testing modules 118a to 118c are mounted onto arbitrary positions, it is possible to control the connections of the inputs and outputs of the trigger controlling modules 114a to 114c and the clock controlling modules 116a to 116c easily and accurately. Accordingly, since no management tale for managing the connections of the inputs and outputs of the trigger controlling modules 114a to 114c and the clock controlling modules 116a to 116c or testing program in response to the mounting positions of the testing modules 118a to 118c is necessary to be prepared in contrast to the testing apparatus related to the prior art, the time required to test the devices under test 150a to 150c can be reduced.

Although the present invention has been described by way of exemplary embodiments, it should be understood that those skilled in the art might make many changes and substitutions without departing from the spirit and the scope of the present invention which is defined only by the appended claims.